Brandon Ardisson

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YOE: 7 years of experience as an electrical engineer. My current role has been focused on digital systems design and custom HDL/RTL module development for networking products. Prior experience in RF design of software defined radio (SDR) communications and sensing systems. Additional experience in custom IC integration, systems modeling, kernel, bootloader, and device driver development for custom hardware.

Education

Arizona State University
Master of Engineering: Electrical Engineering; 2021-2024
Digital Signal Processing & ASIC/FPGA Design; Cumulative GPA: 3.5/4.0

University of Illinois at Chicago
Bachelor of Science in Electrical Engineering; 2015 – 2018
Cumulative GPA: 3.7/4.0

Professional Experience

Ubiquiti Networks (NYSE: UI)
FPGA Design Engineer May 2023 – Present

FPGA Team Lead, and lead developer, for Ubiquiti's Chicago Design Center. We are comprised of a small, agile team that provides focused hardware acceleration solutions and technical leadership to Ubiquiti product teams. High level responsibilities include architecture and design of prototype FPGA systems that meet program performance, risk, cost, and timeline. I also manage junior FPGA team members, coordinate resources and lead code reviews.

Technical contributions include the design and implementation of custom RTL modules, testbench and software development. I regularly perform design verification, timing closure, throughput & latency analysis, resource impact and scaling surveys. Knowledgeable of memory and bus architectures, standard high speed and vendor specific interfaces, with recent projects centered around PCIe and Ethernet. Experience with hardware bring-up, debugging, design for test, first integrator roles, and many other product development centric skills.

I have lead CI/CD process improvements for the FPGA development framework and contributed to creating a collaborative team environment with communication and openness to different perspectives and new ideas. Proficient in System Verilog (some VHDL), C/C++, Python, TCL, Linux shell scripting; but also, always learning!

Motorola Solutions – Applied Technology: Custom Products (NYSE: MSI)
RF Design Engineer May 2017 – May 2023

Responsible for system architecture, design, characterization, and testing of multi-band RF communications circuits/lineups. Involved in all stages of the project lifecycle, from initial concept and prototype, design, test, characterization, manufacture ramp, and delivery. Tasks include architecture design, lineup analysis, component selection, filter design, schematic capture, PCB layout, simulated circuit/layout analysis using Keysight ADS and CST Microwave Studio. Emphasis is

placed on low SWaP architectures, quickly solving challenging design problems, and delivering products of superior quality.

- My contributions to data acquisition, analysis, and project testing efforts led to IP disclosures for MSI
- Lead Electrical on several HDI designs including high frequency > 20 GHz
- High level system planning, link budget, trade studies
- Experience with state-of-art RF hardware and PCB technologies
- Python development for equipment automation and component/hardware test
- Some experience in power amplifier design (Knowledgeable of optimum IMN/OMN for desired amplifier characteristics, load pull, PAE, CCDF, PAPR, performance deltas when using various waveform modulation)

Independent Research

Ardisson, B. (2023). *Applications of Rényi Entropy in Time-Frequency Representation Analysis and Signal Classification*. Unpublished.

Ardisson, B. (2021). *An Analysis of Wide Bandwidth Fixture De-Embedding Achievable Through Use of a Single Calibration Structure.* Unpublished.

Additional experience and research information available here: https://thatrtlguy.com/